IN THE CLAIMS

1. (Currently Amended) A programmable logic device, comprising:

an internal three-statable bus having conductors;

a plurality of interface logic having at least one logic control signal, each of the plurality of interface logic comprising at least one driving element, wherein the at least one driving element is configured to couple to the conductors of the internal three-statable bus, wherein the at least one driving element is operable to drive the internal three-statable bus, and wherein the at least one driving element is coupled to the at least one logic control signal of the plurality of interface logic.

~~a plurality of driving elements coupled to the internal three-statable bus, each driving element operable to drive the internal three-statable bus; and~~

~~a plurality of interface logic circuits, each of the plurality of interface logic circuits coupled to a different one of the plurality of driving elements, each interface logic circuit operable to determine whether the internal three-statable bus is being driven, the interface logic circuits collectively operable to prevent contention of signals on the internal three-statable bus~~.

2. (Currently Amended) The programmable logic device of claim 1, further comprising support circuitry coupled to the internal three-statable bus and the ~~plurality of driving elements~~ at least one driving element.

3. (Original) The programmable logic device of claim 2, wherein the support circuitry comprises:

a different set of drivers for each driving element, wherein each of the plurality of interface logic circuits is coupled to a different one of the set of drivers.

4. (Original) A programmable logic circuit, comprising:

a plurality of logic array blocks, wherein each of the plurality of logic array blocks comprises:

a plurality of logic cells each having a plurality of inputs and an output, and a plurality of interconnect conductors selectively coupled to the plurality of inputs and the output of each of the plurality of logic cells, the plurality of interconnect conductors comprising:

a first type of conductor to couple to more than one logic cell output; and a second type of conductor to couple to a single logic cell output; and

a plurality of multiple spans of conductors coupled to the plurality of logic array blocks and circuit input/output terminals.

5. (Original) An electronic system, comprising:

a processing unit;

the programmable logic circuit of claim 4;

a memory unit to store data;

an interface; and

a bus network to provide communication links between the processing unit, the memory unit and the interface.

6. (Original) The electronic system of claim 5, wherein the processing unit is operable to configure the programmable logic circuit.

7. (Currently Amended) A method, comprising:

driving an internal three-statable bus using at least one ~~of a plurality of~~ driving ~~elements;~~ element of an interface logic; and

coupling the at least one driving element to at least one logic control signal of the internal three-statable bus.

~~determining whether the internal three-statable bus is being driven using at least one of a plurality interface logic circuits, each of the plurality of interface logic circuits coupled to a different one of the plurality of driving elements~~.

8. (Currently Amended) The method of claim 7, further comprising ~~preventing contention of~~ selecting signals on the internal three-statable bus collectively using ~~the~~ a plurality of interface logic circuits.

9. (Currently Amended) The method of claim 8, ~~wherein driving~~ further ~~comprises~~ comprising driving the internal three-statable bus using ~~the plurality of~~ additional driving elements.

10. (Currently Amended) The method of claim 9, ~~wherein determining~~ further ~~comprises~~ comprising determining whether the internal three-statable bus is being driven using the plurality of interface logic circuits.